REMARKS/ARGUMENTS

In the Office Action mailed on January 7, 2009, claims 1-12 are rejected. Additionally, claims 1-12, the drawings, and the specification are objected to. In response, claims 1-12 have been amended and new claims 13-15 have been added. Applicants hereby request reconsideration of the application in view of the claim amendments, the new claims, and the below-provided remarks.

Objections to the Drawings

The Office Action states that elements in Figures 1-5 are not labeled with descriptive text labels. The current application is a U.S. National Stage application. The labeling of figures with text matter is prohibited, except when absolutely indispensible for understanding (see PCT Rule 11.11). Further, MPEP 1893.03(f) states that "[t]he USPTO may not impose requirements beyond those imposed by the Patent Cooperation Treaty (e.g., PCT Rule 11)." Additionally, the elements in Figures 1-5 are labeled with reference numbers and are described in Applicants' specification. Thus, descriptive text labels for the elements in Figures 1-5 are not absolutely indispensible for understanding. In view of the above, Applicants respectfully assert that descriptive text labels for the elements in Figures 1-5 are not required in the current application.

Thus, Applicants respectfully request that the objections to the drawings be withdrawn.

Objections to the Specification

The specification is objected to because the abstract does not commence on a separate sheet in accordance with 37 C.F.R. 1.52(b)(4). The current application is a U.S. National Stage application. It is improper for the Examiner of the U.S. national stage application to require the applicant to provide an abstract commencing on a separate sheet if the abstract does not appear on a separate sheet in the publication of the international application (see MPEP 1893.03(e)(I)). Because the abstract does not appear on a separate sheet in the publication of the international application of the current

application, Applicants respectfully assert that the abstract does not need to be commenced on a separate sheet.

The specification is also objected to because various sections of the specification are not labeled with the appropriate section heading. Applicants note that the section headings are not required in the guidelines set forth in the MPEP 608.01(a) and, hence, Applicants respectfully decline to amend the specification to include the indicated section headings.

Thus, Applicants respectfully request that the objections to the specification be withdrawn.

Claim Objections

Claims 1-12 are objected to because of informalities. In response, claims 1-12 have been amended to correct the informalities. Thus, Applicants respectfully request that the objections to claims 1-12 be withdrawn.

Claim Rejections under 35 U.S.C. 112

Claims 10 and 12 are rejected under 35 U.S.C. 112. In particular, the Office Action states that there is insufficient antecedent basis for the limitations "the processing circuitry" in claims 10 and 12. In response, claims 10 and 12 have been amended to replace the phrase "the processing circuitry" with the phrase "the signal processing circuitry." Support for the amendment to claims 10 and 12 is found in Applicants' specification at, for example, original claims 1 and 12. Thus, Applicants respectfully request that the rejections to claims 10 and 12 under 35 U.S.C. 112 be withdrawn.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, the Office Action states that it is unclear what the phrase "that particular item of frame data" refers to. In response, claim 3 has been amended to recite in part that "the second video stream processing function is arranged to read each item of frame data from the second buffer memory at respective times, the second video stream processing function being arranged to read a particular item of frame data from the second buffer memory before the first video stream processing function has

written a full frame following that particular item of frame data." Support for the amendment to claim 3 is found in Applicant's specification at, for example, original claims 1 and 3. Thus, Applicants respectfully request that the rejection to claim 3 under 35 U.S.C. 112 be withdrawn.

As a result, Applicants respectfully request that the rejections to claims 3, 10, and 12 under 35 U.S.C. 112 be withdrawn.

Claim Rejections under 35 U.S.C. 102

Claims 1-12 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Okada (U.S. Pat. No. 6,871,001 B1). As described above, claims 1-12 have been amended to overcome claim rejections and claim objections. Additionally, new claims 13-15 have been added. Applicants respectfully submit that the pending claims are not anticipated by Okada for the reasons provided below.

Independent Claim 1

Claim 1 recites in part:

> "the second video stream processing function being arranged to select to read the frame data of predetermined first and second ones of the frames selectively from the first and second buffer memory respectively, the second ones of the frames occurring in the same temporal order in both the input and output sequence, the first ones of the frames containing at least all particular frames whose position relative to the second ones of the frames in the output sequence differs from the position of the particular frames relative to the second ones of the frames in the input sequence." (emphasis added)

That is, claim 1 recites that a signal processing circuitry reads frames from a second buffer memory in a sequence in time, which sequence in time is the same sequence in time as the frames were written into the second buffer memory. Additionally, claim 1 recites that the signal processing circuitry also reads frames from a first buffer memory in a sequence in time, which sequence in time is different from the sequence in time as the frames were written into the first buffer memory. Applicants respectfully assert that Okada fails to disclose the above-described limitations of claim 1.

With reference to Fig. 1, Okada discloses that an MPEG decode core circuit (105) receives video streams stored in frame buffers (104a) and (104b), see also column 8, lines 33-42. In particular, Okada discloses that the MPEG decode core circuit (105) receives

video streams stored in the frame buffers (104a) and (104b) through different paths and outputs the processing results back to the frame buffers (104a) and (104b) through different paths, see Fig. 1, column 8, lines 49-61, the paragraph between column 8, line 62 and column 9, line 3, and column 9, lines 4-12. Okada also discloses that a display circuit (107) generates a video signal from picture data from the frame buffers (104a) and (104b) and outputs the video signal to an external device (131), see column 9, lines 31-43.

Although Okada discloses generating a video signal from data written into the frame buffers (104a) and (104b), it is silent as to the relationship between the sequence in which the data was written into the frame buffers and the sequence in which the data was subsequently read from the frame buffers. In particular, Okada fails to disclose that the display circuit (107) reads frames from one of the frame buffers (104a) and (104b) in, which sequence in time is the same sequence in time as the frames were written into the frame buffer. Okada also fails to disclose that the display circuit (107) reads frames from the other frame buffer of the frame buffers (104a) and (104b) in a sequence in time, which sequence in time is different from the sequence in time as the frames were written into the frame buffer. Accordingly, Okada fails to disclose the above-identified limitations of claim 1.

Because Okada fails to disclose the above-identified limitations of claim 1, Okada fails to disclose all of the limitations of claim 1. Thus, Applicants respectfully assert that claim 1 is not anticipated by Okada.

Dependent Claims 2-10

Claim 6 has been further amended to replace the phrase "the first video stream processing function" with the phrase "the signal processing circuitry." Support for the amendment is found in Applicants' specification at, for example, original claims 1 and 6. Claims 2-10 depend from and incorporate all of the limitations of independent claim 1. Thus, Applicants respectfully assert that claims 2-10 are allowable at least based on an allowable claim 1. Additionally, claims 2, 3, and 6 may be allowable for further reasons, as described below.

Claim 2 recites in part "*a first integrated circuit, which comprises the signal processing circuitry and the second buffer memory, and a second, separate integrated circuit that comprises the first buffer memory*" (emphasis added). Applicants respectfully assert that Okada fails to disclose the above-identified limitation of claim 2. In particular, Okada discloses that the frame buffers (104a) and (104b) and the MPEG decode core circuit (105) of an MPEG video decoder (1) are located on one LSI chip, see column 7, line 65-66. Because Okada discloses that the frame buffers (104a) and (104b) and the MPEG decode core circuit (105) are located on a single chip, Okada fails to disclose that one of the frame buffers (104a) and (104b) is located on separate integrated circuit from the MPEG decode core circuit and the other frame buffer, as recited in claim 2.

Claim 3 recites in part "*the second video stream processing function being arranged to read a particular item of frame data from the second buffer memory before the first video stream processing function has written a full frame following that particular item of frame data*" (emphasis added). Applicants respectfully assert that Okada fails to disclose the above-identified limitation of claim 3. In rejecting claim 3, the Office Action refers to column 8, lines 56-61 and column 9, lines 4-12 of Okada. Column 8, lines 56-61 of Okada discloses that when a switch circuit (3) is switched to a node (3b) side, the processing result from an MPEG decode core circuit (105) is transferred in a sequence through a buffer (114b), a data bus (106b), a memory controller (108b), and output to the frame buffer (104b). Column 9, lines 4-12 of Okada disclose that data from the frame buffer (104b) is read by the memory controller (108b), transferred in a sequence through the data bus (106b) and the buffers (111b-113b), and input to the MPEG decode core circuit (105). That is, column 8, lines 56-61 and column 9, lines 4-12 of Okada disclose sequences of transmission between the MPEG decode core circuit (105) and the frame buffer (104b). Column 8, lines 56-61 and column 9, lines 4-12 of Okada fail to disclose that a particular item of frame data is read before a full frame has been written following that particular item of frame data.

Claim 6 recites in part that "*the signal processing circuitry writes B frames to the second buffer memory only*" (emphasis added). Applicants respectfully assert that Okada fails to disclose the above-identified limitation of claim 6. In particular, Okada discloses

that a B-Picture is stored in both the frame buffer (104a) and the frame buffer (104b), see column 9, lines 26-29.

Independent Claim 11

Claim 11 includes similar limitations to claim 1. Because of the similarities between claim 11 and claim 1, Applicants respectfully assert that the remarks provided above with regard to claim 1 apply also to claim 11. Accordingly, Applicants respectfully assert that claim 11 is not anticipated by Okada.

Independent Claim 12

Claim 12 includes similar limitations to claim 1. Because of the similarities between claim 12 and claim 1, Applicants respectfully assert that the remarks provided above with regard to claim 1 apply also to claim 12. Accordingly, Applicants respectfully assert that claim 12 is not anticipated by Okada.

New Claims 13-15

Claims 13-15 have been added. Support for claims 13-15 is found in Applicants' specification at, for example, page 5, lines 20-23. Claims 13-15 depend from and incorporate all of the limitations of independent claims 1, 11, and 12, respectively. Thus, Applicants respectfully assert that claims 13-15 are allowable at least based on allowable claims 1, 11, and 12, respectively. Additionally, claims 13-15 may be allowable for further reasons, as described below.

Claims 13-15 recite in part that "*the second buffer memory has a capacity of less than one frame*" (emphasis added). Applicants respectfully assert that Okada fails to disclose the above-identified limitations of claims 13-15. In particular, Okada discloses that each of two frame buffers (104a) and (104b) stores a B frame, a future I or P frame, and a past I or P frame, see Fig. 1 and column 9, lines 14-19. Because Okada discloses that each of two frame buffers (104a) and (104b) stores multiple frames, Okada fails to disclose that any of the frame buffers (104a) and (104b) has a capacity of less than one frame. Thus, Applicants respectfully assert that Okada fails to disclose the above-identified limitations of claims 13-15.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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